Fan Out – Simple to Complex

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2000 – A Revolution Occurred in OSAT Packaging

Packaging Technologies

Package Focused
- Mechanical Processes
  - Grinding
  - Sawing
  - Die Bonding
  - Wire Bonding
  - Molding
  - Singulation

+ Wafer Focused
- Chemical Processes
  - Wafer Processing
  - Sputtering
  - Plating
  - Etching
  - Plasma
  - Photo Processing
    - Photoresists
    - Polymers
Evolution of New Technologies

- OSAT Wafer Level Processing
- Bumping
- WLCSP
It Started in 2001
Wafer Level Enabled New OSAT Packaging...

- Bumping 2000
- WLCSP 2001
- WL IPD 2005
- WL MEMS 2008
- WL Fan Out 2009
- 3D Fan Out 2011
- HD Fanout 2014
- FOPoP 2016
- FOSiP 2017
**Fan In Package? Fan Out Package?**

**“Fan In”**
All RDL traces are routed in towards the center of the die

**“Fan Out”**
RDL traces are routed both in and outwards beyond the limits of the die
Drivers for Fan Out

- **Die Shrinkage**
  - Fan Out allows ball placement beyond die area

![WLCSP](image1) ➔ ![FOWLP](image2)

- **Heterogeneous & Homogeneous Integration**
  - Excellent electrical connectivity

![Heterogeneous Integration](image3)

- **System in Package (SiP)**
  - Interconnect wide variety of components
  - Small Size

![SiP](image4) ➔ ![Fan Out SiP](image5)
Two Primary Fan Out Structures/Processes

Chip First

Chip Last
Chip First vs Chip Last Fan Out

**Chip First Fan Out**

1. Wafer Dicing
2. Wafer Reconstitution
3. Molding
4. RDL Formation
5. Backend

**Chip Last Fan Out**

1. Wafer Bumping
2. Wafer Dicing
3. Trace & Pad Formation
4. Flip Chip & Molding
5. Backend

[Images of process flow for Chip First and Chip Last Fan Out]
Subdivide Fan Out into Two General Categories

- **Low Density (LD) Fan Out**
  - Less than ~ 500-600 I/O
  - Lines/Spaces $\geq 8\mu m$

- **High Density (HD) Fan Out**
  - Greater than ~ 500-600 I/O
  - Lines/Spaces $< 8\mu m$
Low I/O, L/S >= 8µm

Early Applications
– Baseband & RF Transceiver

New Opportunities – Varied Applications
- 24/77GHz Automotive Radar
- Automotive
- Medical
- PMIC
- mm Waveband
- Ultrasound
- DRAM & NAND Memory
- MEMS
- Sensors
- RF Connectivity
- NFC Chips
- WIFI
- Bluetooth
- GPS

- DC/DC Converters
- CODECS
- IPDs
- Audio
- Analog
- Touch IC Controllers
- LCD Display Drivers
- PA Modules
LD Wafer Level Fan Out Variations

- Chip First Die Down
- Chip First Die Up
- Chip Last (Panel)
- Chip Last (Wafer)
Evolutionary Paths for eWLB
Chip First Die Down vs Die Up?

- Mold compound allows additional spacing between the die and RDL traces & UBM and potentially better high frequency electrical performance
- Mold compound over die provides better buffering for Chip Package Interaction

**Chip First Die Down**
- eWLB

**Chip First Die Up**
- Deca M-Series

M-Series Has 5X larger Standoff vs eWLB

Drawings are shown to scale
HD Fan Out Opportunities

- High I/O, L/S <8µm
- Package on Package Applications (POP)
- System in Package Applications (SiP)
- Opportunities – Varied Applications
  - APU + Memory
  - GPU + Memory
  - Network Applications
  - SiP/ Modules
HD Wafer Level Fan Out Variations

**Chip First Die Down**
- HD eWLB
- FOCoS – Hybrid Fan Out Chip on Substrate (FO FCBGA)

**Chip First Die Up**
- HD FO
- HD FOPoP
- HD FOPoP with RDL
- HD FOPoP SiP

**Chip Last**
- Chip Last Single Sided SiP
- Chip Last Double Sided PoP SiP
- Chip Last Double Sided PoP SiP w/RDL
FOCoS
Fan Out Chip on Substrate
High Density 2.1D Fanout – 2.5D Alternative

- Organic 2.1D Interposer Applications
  - APU + Memory
  - GPU + Memory
  - Network Applications
  - SiP/Modules

- Hybrid Solution
- Combines HD Fan Out with FCBGA
- High Density 2D & 3D Interconnection in RDL Layers, no need for interposer
- Most Complex Fan Out in Production
- Requires Advanced Fan Out & Advanced FlipChip Assembly

- 2/2.5μm L/S
- 3 RDL Layers + UBM
- 16 & 28nm Die
- 24x26mm FO
- 45x45mm Package

Multiple Products in Volume Production since January 2016
FO on Substrate can Replace 2.5D

- Fan Out can replace 2.5D/Interposer for specific applications
FOCoS Variations

- FOCoS Chip First Die Down

- FOCoS Chip Last
FOCoS Production Cross Sections
FOCoS Production Cross Sections
High Density Chip First Die Up

POP Fan Out

3D Fan Out Logic Bottom Package + Memory Package = Assembled Fan Out POP
Fan Out PoP
Fan Out POP
High Density Chip Last Wafer Fan Out

Chip Last Single Sided SiP

Chip Last Double Sided POP SiP

Chip Last Double Sided POP SiP w/RDL
ASE Fan-out Package Platform

eWLB
- BB, RF, Codec, PMIC
- Max. Pkg size ~12x12
- RDL L/S > 8/8um
- 2L RDL
- Production
- 180+M units shipped since Y2009
- Chip first - Wafer
- Die down
- Original FO in volume production
- Low & Medium Density I/O
- Multi-Die & Passives

FOCLP
- BB, RF, Codec, PMIC
- Max. Pkg size ~12x12
- RDL L/S > 12/12um
- 2L RDL
- Production
- 100M+ units shipped since Y2014
- Chip last - Panel
- Cu pillar on die
- Very thin Coreless substrate
- Multi die + Passives
- Same form factor as eWLB

FOCoS
- Fan Out Chip on Substrate Networking, Server
- Max. Pkg size ~45x45
- RDL L/S => 2/2um
- 3L RDL, 4 Metal
- Production
- >800K units shipped since Jan 2016
- Chip first - Wafer
- Die down Hybrid
- Fan Out Bumped pseudo-die ~12,000 I/O
- FC BGA Assembly
- Die to Die >1000 I/O
- Alternative to 2.5D
- Multi-Die & Passives

M-Series
- BB, RF, Codec, PMIC
- Max. Pkg size ~12x12
- RDL L/S > 8/8um
- 2L RDL MultiDie
- Qualification
- Production
- >800K units shipped since Jan 2016
- Chip first - Wafer
- Die up
- Deca Process
- Low & Medium Density I/O
- Multi-Die
- Wafer Panel Development

FOPoP
- AP & Memory Integration
- Chip first/Last - Wafer
- Die up
- Cu pillar on die
- Known good RDL
- Low & Medium Density I/O
- Multi-Die
- Qualification
- Engineering
- Hundreds built, In Qualification

FOSiP
- AP & Memory Integration, RF Module
- Max. Pkg size ~15x15
- RDL L/S => 5/5um
- 3L RDL
- Engineering
- Hundreds built

Chip last - Wafer FO
- Known good RDL
- Die shift/warpage controlled
- High cure dielectric available
- Multi-Die & Passives
Fan In to Fan Out – 2D to 3D

- eWLP FO Die Down
- M-Series FO Die Up
- Panel FO Chip Last
- Hybrid FO/BGA Die
- Chip Last FO SiP
- FO POP w/o Top RDL
- WLCSP
- FO POP w/Top RDL
- FO Chip Last w/o Top RDL
- FO Chip Last w/Top RDL
- FO POP w Memory
- 2D
- 2.1D
- 3D

Source: SEMICON TAIWAN
Summary

- **New Packaging Innovations improve**
  - Cost
  - Miniaturization
  - Performance
  - SiP

[Diagram showing WLCSP, Fan Out Package, 3D Fan Out Package on Package, 3D FO System in Package]