Transforming Electronic Interconnect

Breaking through historical boundaries

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Deca Technologies
Remember when?
There were three distinct industries
Wafer Foundries

Semiconductor Devices
Nanometers

SATS
Packaging
10’s of Microns

EMS
Electronic Systems
100’s of Microns
Wafer Foundries

1.5 microns

SATS

15 microns

EMS

150 microns
Wafer Foundries

SATS

EMS
Convergence of industries

Characteristics of Convergence

• Electroplated Cu interconnect
• Photo-imageable dielectrics
• Multi-level routing layers
• Large area format processing
• Direct connection to active Si
• Large overlap in routing dimensions
Coming from different historical financial models

Capital Intensity
(Annual capex ÷ Annual revenue)

Gross Margin%
Leading Foundry
Leading SATS Providers
Leading EMS

Operating Income%
Leading Foundry
Leading SATS Providers
Leading EMS
# Producing significantly different cost levels

<table>
<thead>
<tr>
<th><strong>Foundries - Device Level Electronic Interconnect</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td><strong>Typical Geometries</strong></td>
</tr>
<tr>
<td>Digital processor</td>
<td>10 nm</td>
</tr>
<tr>
<td>Analog</td>
<td>28 to 150nm</td>
</tr>
<tr>
<td>RF</td>
<td>55 to 180nm</td>
</tr>
</tbody>
</table>

**SATS - 1ˢᵗ Level Elec. Interconnect**

Flip chip CSP packaging

**Typical Cost**

0.7¢ per mm²

**EMS - 2ⁿᵈ Level Elec. Interconnect**

10 layer Smartphone motherboard

**Typical Cost**

0.5¢ per mm²
Producing significantly different cost levels

Technology Cost Comparison
(Sales price to customers)

<table>
<thead>
<tr>
<th>Technology</th>
<th>Cents per mm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adv Si</td>
<td>6</td>
</tr>
<tr>
<td>RF Si</td>
<td>4</td>
</tr>
<tr>
<td>Analog Si</td>
<td>3</td>
</tr>
<tr>
<td>FC CSP</td>
<td>0.7</td>
</tr>
<tr>
<td>OEM PCB</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Classic electronic interconnect technology gap
What if?

• Advanced wafer fab BEOL (Back End Of Line) interconnect

Source: Reverse Costing Analysis – Apple A10 with TSMC’s inFO packaging, iPhone 7 Plus Application Processor, SYSTEMPlus Consulting, September 2016

• Could be produced in a different way?

With large panel fan-out technology
M-Series fan-out technology

Chips first, chips up fan-out with fully encapsulated active region

Planar patterning surface with roadmap to 2µm line & space

Adaptive patterning to enable high yields in scaling to tight geometries & low cost die attach

Improved reliability with embedded silicon and molded stress buffer

Cost-effective solar wafer fab inspired Autoline equipment for 300mm & large panel formats

Note: Multiple patents granted & pending
M-Series building blocks

Multi-Layer, multi-thickness RDL & Dielectrics

Direct Connect Thick Cu
Low contact resistance, multi-via capture

Polymer Isolated Via
Further stress isolation, tighter design rules

5µm lines

5µm Nested Lines

5µm Isolated Line
Breaking through the barriers

Capital cost breakthrough

SUNPOWER
Solar wafer fab inspired approach
‘Non-fab equipment set’

Yield & cost breakthrough

Adaptive Alignment*
Align the entire RDL pattern to the measured die position

Adaptive Routing*
Dynamically adapt RDL routing to the measured die position

Adaptive Patterning™
Aligns the entire RDL pattern to the measured die position

Enables high metal density designs
Precisely aligns inductors to the die

BGA array fixed to package outline
Enables multi-die fan-out

*Note: Multiple patents issued & pending
M-Series Adaptive Patterning

Dual-die application example
- High frequency SoC
- Bluetooth radio

Adaptive Patterning enables precise fixed pattern alignment for RF devices & adaptive routing for 100% yield for multi-die interconnect

Adaptive alignment for RF
Adaptive routing for 100% yield
Moving from 300mm round to large panel fan-out

Wafer Processing Cost
300mm round baseline*

- Depreciation
- Materials
- Labor
- Fac, Ovhd, Other

*Estimated industry average COGS of M-Series with Adaptive Patterning

Large panel fan-out has the potential for >30% cost reduction
- Capital productivity
- Material efficiency

Estimated capital to install 30k per month capacity
(300mm round panel equivalent)

Panel area in k mm²

- 70.7
- 90
- 159
- 180
- 250
- 262
- 360

*Equivalent edge dimension if square
Convergence through M-Series large panel fan-out

Technology Cost Comparison
(Sales price to customers)

- **Adv Si**: 6 cents per mm²
- **Analog Si**: 3 cents per mm²
- **RF Si**: 2 cents per mm²
- **FC CSP**: 0.7 cents per mm²
- **OEM PCB**: 0.5 cents per mm²

M-Series large panel fan-out potential
Fan-out Applications → Blurring the Lines

Wafer Foundries

- SoC Disintegration
  - Apps processor
  - BB Modem
  - RF Combo

SATS

- Single Die Packaging
  - PMIC
  - RF Transceiver
  - Audio Codec

EMS

- EMS-like Modules
  - Wide IO & HB Memory
  - Multi-function RF
  - PoP
Convergence of industries

Through M-Series fan-out technology
Convergence through large panel M-Series fan-out

Initial Production

- 300mm round
- M-Series Structure*

Future Production

- (post chip attach)
- (post mold & debond)

Large panel format M-Series*

*Note: Multiple patents issued & pending

... in cooperation with ASE
Thank You