Panel Level Embedding for Power and Sensor Applications

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Outline

- Introduction  Panel-level Packaging
- PLP in Manufacturing
- PLP at Fraunhofer IZM
- PLP Applications
  - Power
  - Camera
- Conclusions
Today's Packaging

Leadframe Packaging  Strip Packaging  Wafer-level Packaging

Fan-out Wafer-level Packaging

Need for further cost reduction
→ Increase of production format size
Evolution of FO WLP towards Panel-Level Packaging (PLP)
From Wafer Size to Panel Size

**PCB Technologies**

- Based on standard PCB materials & equipment
- 3D and double sided routing are standard features for PCBs
- Line/space down to 10 µm
- Full format/large area is standard

**Thin Film Technologies**

- Based on standard thin film technology equipment
- Tightest tolerances for fine pitch line/space (2/2 µm)
- Currently limited to 12” – 300 mm

![Diagram showing wafer sizes 8" and 12", and panel sizes 24"x18" and 24"x24".]
Panel-Level Packaging - PLP

**Definition:**
Throughout manufacturing of packages on large formats

**Features**
- Lead-less package (BGA, QFN, LGA)
- Embedded components (active and passive)
- Components on top
- High-density interconnects
- 3D capability
- Rectangular or square production formats 18” - 24” or larger
Technologies for Panel-Level Packaging

→ Fusion of different technologies

Leadframe/ Strip Format

die attach
materials and processes

Wafer-Level FO Wafer-Level

mold technology & materials / through mold vias
thin film materials / sputtering

LCD Technology

equipment for very large area
• polymer application
• metal sputtering

PCB Technology Embedding

advanced PCB processes & materials read for PLP
improvement resolution and accuracy for next Gen PLP

Fraunhofer IZM
Challenges for PLP Processes

Warpage (⇒ Assembly, Manufacturability)
- heterogeneous materials and non-symmetric structures cause bow
- polymer materials with adapted CTE, modulus and low shrink are required
- optimized layer sequence and design required

Accuracy/Resolution (⇒ Miniaturization)
- improved optical recognition systems for placement equipment
- imaging with high depth of focus and high resolution
- local alignment ⇒ LDI or stepper

Yield (⇒ Cost)
- suited materials and components
- optimized processes
- production experience ⇒ Learning Curve
Panel-Level Packaging in Manufacturing today
Embedded Component Packaging (ECP)
Embedded Component Packaging (ECP)

ECP® Volume production experience

<table>
<thead>
<tr>
<th>Month</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>March 2009</td>
<td>First Contact</td>
</tr>
<tr>
<td>May 2009</td>
<td>Prototyping</td>
</tr>
<tr>
<td>Sept 2009</td>
<td>Reliability Testing</td>
</tr>
<tr>
<td>April 2010</td>
<td>Production Ramp Up</td>
</tr>
<tr>
<td>Sept 2010</td>
<td>Customer Audits</td>
</tr>
<tr>
<td>April 2011</td>
<td>Dedicated Organisation</td>
</tr>
<tr>
<td>May 2011</td>
<td>Volume Production</td>
</tr>
<tr>
<td>Now</td>
<td>Millions of Shipped Units</td>
</tr>
</tbody>
</table>

“We are audited and approved to the highest standards. ECP® is ready for your requirements today”

- Units shipped: ca. 200 Mio
- AT&S Yield: > 99.5%
- Field returns: 0

courtesy AT&S
Embedded Component Packaging (ECP)
Semiconductor Embedded in Substrate (SESUB)
Blade Package

SMD power package

- embedded MOSFET / Driver
- manufacturing on PCB format

Licensing and process transfer from Fraunhofer IZM
Panel-Level Packaging at Fraunhofer IZM

- R&D for Future Products
PLP Strategies

Panel-Size FO WLP

- Large-area molding 18" x 24"
- Through mold vias for 3D
- Interconnects using PCB materials & technology
- Mold embedding of sensors

PCB Embedding

- Use of new polymers / laminates
  - Thin layers (10 µm) for high density
  - High breakthrough (>40 kV/mm) for power
- Improved resolution for interconnects
  - 10 µm → 5 µm → 2 µm
- Processes to reduce warpage
Fraunhofer IZM Substrate Integration Line

- High-end manufacturing equipment dedicated to customer-specific R&D
- Complete 18" x 24" PCB manufacturing & assembly line

- Laser, drilling, lamination: 400 m²
- Lithography (LDI), sputtering, galvanics, etching: 280 m²
- Assembly, molding, analytics: 100 m²
- 40 scientist, engineers and technicians with long-term experience in advanced packaging

Total area: 1120 m²
Fraunhofer IZM Substrate Integration Line

**Placement**
- Datacon evo/ASM Siplace CA3

**Accuracy**
- Mahr OMS 600/IMPEX proX3

**Molding**
- WL: Towa up to 8”
- PL: APIC up to 18”x24” incl. 12” WL (Q3 – 2014)

**Lamination**
- Lauffer/Bürkle

**Laser Drilling**
- Siemens Microbeam/Schmoll Picodrill with HYPER RAPID 50

**Mech. Drilling**
- Schmoll MX1

**Cu Plating**
- Ramgraber automatic plating line

**Imaging**
- Orbotech Paragon Ultra 200

**Etching**
- Schmid
Assembly of 5528 dies on large area 18”x 24” with 6500 dies/h speed

Mold embedding on large area 18”x 24” by sheet lamination

Fully electrical connected WL embedded package stack with TMV & 3D routing

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Panel Molding 18”x 24” – APIC Yamada

Equipment in Japan before shipment

First molded panel 18" x 24 "

Large area compression molding:
- Wafer Level: 300 mm up to 450 mm possible
- Panel Level: 18” x 24” (456 x 610 mm²)
- Lamination

Up and Running in Q4/2014
Panel-Level Packaging for Power Applications
PCB Embedding Today – Power and Logic

The production of embedded packages is ramping up fast

Smart Phone Market
• DC/DC converters
• Power management units
• Connectivity module

Computer market
• MOSFET packages
• Driver MOS SiPs

PCB Embedding Technology is implemented or will come soon at
• PCB manufacturers
• Semiconductor manufacturers
• OSATS
Power Chip Embedding - Features

- Embedding of power chips into Printed Circuit Board structures
  - cost saving by large area process ➔ PLP
- Direct connection by Cu conductors / no bond wires
  - high reliability by direct Cu to chip interconnects
  - shielding capability
- Completely planar conductors
  - multiple wiring layers possible
  - SMD assembly on top allows driver integration
  - top side cooling possible
  - very low parasitic effects
Power Chip Embedding – Manufacturing Process

- backside contact by conductive die bond
  - conductive adhesive
  - soldering
  - sintering
- very good thermal conductivity
- die attach on thick Cu possible
- compatible to standard Ag backside

embedding by lamination

via drilling top, through-via

Cu plating and structuring

Ag sintered die bond
Ultra Low Inductance Package for SiC

Best Paper of PCIM 2013 Conference

- Full bus bar structure using PCB Process on a DBC
- DC capacitors on the module
- DC link current measurement included

Package sets new benchmark:

⇒ ultra-low DC-link inductance
Ultra Low Inductance Package for SiC

- Switch off at 20 A:
  Voltage slope 19 V/ns
  current slope max. 4 A/ns
  (50% to 90%)
- Low overshot (appr. 10 V)
- very little ringing
  (frequency 240 MHz)

0.8 nH DC-link inductance
Future Perspective – Power Electronics Packaging

- Wire-bonded power chips on DCB
- Planar packages & module with embedded power chips

Traditional Power modules

- Single module manufacturing

Planar Power Packaging

- Large panel manufacturing
  - Low inductance
  - High heat transfer
  - High integration level
  - High productivity

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Panel-Level Packaging for Sensor Applications
MoMiCa – Modular Camera Module

**Motivation**
- to develop a miniaturized camera module with integrated image processing
- using PCB PLP embedding

**Potential Applications**
- traffic lane recognition
- face / gender recognition
MoMiCa – Camera Module

Geometry
• 16 x 16 x 3.6 mm³, weight 2 g w/o lens

PCB Layers
• 2 + 8 + 1 construction
• 8 layer core with stacked microvias

Embedded Components
• 32 bit microcontroller with image sensor interface (CogniVue CV2201 BGA 236)
• 256 Mbit Flash Memory (Macronix 8WSON)
• MOSFET switch (IRF SOIC)
• USB ESD protection (NXP SOT457)
• 5 DC/DC-converters (Murata)
• oscillator 24 MHz (NXP)
• 2 LEDs (0402)
• 34 capacitors (0201, 0603)
• 25 resistors (0201)
• 3 inductors (0603)

Components on top
• 3 MPixel Image Sensor Omnivision 3642
• lens CMT746 + lens holder
• 7 capacitors (0201)
• 1 resistor (0201)
• 1 inductor (0603)
• 1 microswitch
MoMiCa - Layer Sequence

- SMD Bildsensor
- 2 Lagen Kern
- Bauelemente
- 3 Build-up Lagen
- 2 Lagen Kern
- 3 Build-up Lagen
- Bauelemente
- Außenlage
MoMiCa - PLP Manufacturing

- manufacturing on quarter format (12" x 9")
- 77 modules per panel (only partially with components)
- double-side component assembly on inner layer
- embedding by prepreg lamination
- assembly of image sensor on top
- testing and programming on panel-level

assembled components on bottom inner layer

assembled components on top inner layer

Fraunhofer IZM
MoMiCa – Camera Module

Modular camera with integrated 32 bit image processor and memory

- 3 Mpixel image sensor
- 32 bit microcontroller
- DC/DC converter
- Capacitor
- Flash memory
Conclusions

- Panel-level Packaging will gain a significant market share
- There will be a fusion of different technologies
- FO WLP will evolve towards large panels
- PCB technology will evolve towards very high density
- Power application are first in volume manufacturing

... it just started - take the opportunity!
Thank You